

In the Claims

Please amend the claims as follows:

- 1 1. (Previously Amended) A digital system, comprising:
 - 2 a memory circuit;
 - 3 a first requestor circuit with a first memory access node;
 - 4 a second requestor circuit with a second memory access node;
 - 5 a scheduling circuit connected to the first memory access node
 - 6 and to the second memory access node and having a request output
 - 7 node, operable to sequentially schedule memory accesses to the
 - 8 memory circuit by the first requestor circuit and by the second
 - 9 request circuit;
 - 10 a selection circuit connected to the first memory access node
 - 11 and to the scheduling circuit request output node with an output
 - 12 node connected to the memory circuit;
 - 13 access mode circuitry for indicating at least a first access
 - 14 mode and a second access mode controllably connected to the
 - 15 selection circuit, such that both the first requestor circuit and
 - 16 the second requestor circuit can sequentially access the memory
 - 17 circuit when the access mode circuitry indicates the first access
 - 18 mode and the first requestor circuit has exclusive access to the
 - 19 memory circuit when the access mode circuitry indicates the second
 - 20 access mode; and
 - 21 a size register for holding a size parameter coupled to the
 - 22 selection circuit, the selection circuit being operable to select a
 - 23 first portion of the memory circuit in response to the size
 - 24 parameter when the access mode circuitry indicates the second
 - 25 access mode, wherein only the first portion of the memory circuit
 - 26 is operable for exclusive access by the first requestor when the
 - 27 access mode circuitry indicates the second access mode.

1 2. (Original) The digital system of Claim 1, wherein a
2 second portion of the memory circuit not selected in response to
3 the size parameter is operable to be in a low power mode when the
4 access mode circuitry indicates the second access mode.

1 3. (Original) The digital system according to Claim 1,
2 wherein the selector circuit is operable such that a second portion
3 of the memory circuit not selected in response to the size
4 parameter can be accessed by the second requestor when the access
5 mode circuitry indicates the second access mode.

1 4. (Original) The digital system according to Claim 1,
2 wherein the size parameter is ignored when the access mode
3 circuitry indicates the first access mode such that the entire
4 memory circuit is operable to be selected for sequential access by
5 the first requestor and the second requestor.

1 5. (Original) The digital system according to Claim 1,
2 further comprising a clock circuit connected to the second
3 requestor and to the memory circuit, wherein the first portion of
4 the memory circuit operates synchronously with the clock circuit
5 when the access mode circuitry indicates the first access mode and
6 wherein the first portion of the memory circuit operates in an
7 asynchronous manner when the access mode circuitry indicates the
8 second access mode.

1 6. (Original) The digital system according to Claim 1,
2 wherein the first requester circuit is a host processor and the
3 second requester circuit is direct memory access circuit channel
4 controller.

1 7. (Original) The digital system according to Claim 1 being
2 a cellular telephone wherein one of the requestors is a
3 microprocessor, further comprising:

4 an integrated keyboard (12) connected to the microprocessor
5 via a keyboard adapter;

6 a display (14), connected to the microprocessor via a display
7 adapter;

8 radio frequency (RF) circuitry (16) connected to the
9 microprocessor; and

10 an aerial (18) connected to the RF circuitry.

1 8. (Original) A method of operating a digital system having
2 a memory circuit that is shared by a plurality of requestor
3 circuits, comprising the steps of:

4 sharing access to the memory circuit between the plurality of
5 requestor circuits when the digital system is in a first mode of
6 operation;

7 selecting a first portion of the memory circuit responsive to
8 a size parameter stored in a register, such that a second portion
9 of the memory circuit is not selected; and

10 limiting access to the first portion of memory circuit to only
11 a first requestor of the plurality of requestors when the digital
12 system is in a second mode of operation.

1 9. (Original) The method of Claim 8, further comprising the
2 step of sharing access to the second portion of the memory circuit
3 between the plurality of requestor circuits when the digital system
4 is in the second mode of operation.

1 10. (Original) The method of Claim 8, further comprising the
2 step of placing the second portion of the memory circuit in a low
3 power mode when the digital system is in the second mode of
4 operation.

1 11. (Previously Added) The method of Claim 8, wherein the
2 memory has a total size equal to the sum of the first portion and
3 the second portion.

1 12. (Previously Added) The method of Claim 11, further
2 comprising the step of storing a different size parameter in the
3 register, such that the step of selecting results in a first
4 portion having a different size in response to the different size
5 parameter.